CAVIAR Hardware Interface Standards, Version 2.01

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Abstract

This document defines the bus and interface standard for the parallel AER protocol that has been introduced for the CAVIAR project in 2001. It has mainly been used by ETH Zürich, IMSE in Sevilla, University of Sevilla, and University of Oslo. A number of AER chips, like a temporal contrast retina, a 2D convolution chip, a 2D WTA chip and a competitive spike/rate based Hebbian learning chip have been produced by these groups and may be available from them if requested. In addition there are a couple of tools for injecting, projecting, and monitoring of address events.

1 Physical cable and connector

This section defines the cable and connectors that are used for the AER bus. In the tables that describe the signals and signal blocks the pin numbers are also given in Matlab-notation: $<\mathit{start}>:<\mathit{step}>:<\mathit{stop}>$ or in case $<\mathit{step}>$ is 1: $<\mathit{start}>:<\mathit{stop}>$. Example: 72:-1:65 corresponds to 72, 71, 70, 69, 68, 67, 66, 65. The signal names are, however, also written directly beside the pins in the graphics of the plugs, footprints and chip-padframes.

1.1 ATA/133 cable and connector

It was considered an easy 'off the shelf' solution to use a cable and connector that are widely spread for fast digital signals. We decided to use the ATA/133 standard that uses a 40 pin IDC connector and a 80 line ribbon-cable. It is usually used for data transfer from hard disks in most commercial PCs. The data lines are inter-spaced by ground connected lines for decoupling. Thus the special connectors are distributing the ground pins to every second line in the ribbon cable. (For very short connections normal 40 conductor ribbon cables and IDC connectors may be used.) The signal blocks are described in table 1. The pin assignment in the physical plugs is depicted in figure 1.

AER signal name	description	ATA standard	pin number
Reserved	available to extend standard	/RESET	1
AE[0:15]	AER data	DD[0:15]	17:-2:3, 4:2:18
GND		GND	2, 19, 22, 24, 26, 30, 40
/REQ	AER request	DMARQ	21
/ACK	AER acknowledge	/DMAACK	29
Key-pin, not present		Key-pin, not present	20
Reserved		/DIOW	23
Reserved		/DIOR	25
Reserved		IORDY	27
Reserved		SPSYNC:CSEL	28
Reserved		INTRQ	31
Reserved		/IOCS16	32
Reserved		DA1	33
Reserved		PDIAG	34
Reserved		DA0	35
Reserved		DA2	36
Reserved		/IDE_CS0	37
Reserved		/IDE_CS1	38
Reserved		/ACTIVE	39

Table 1: Signal description of 40 pin IDC connectors according to the consortium's AER bus standard and the corresponding pin names in the ATA/133 standard.

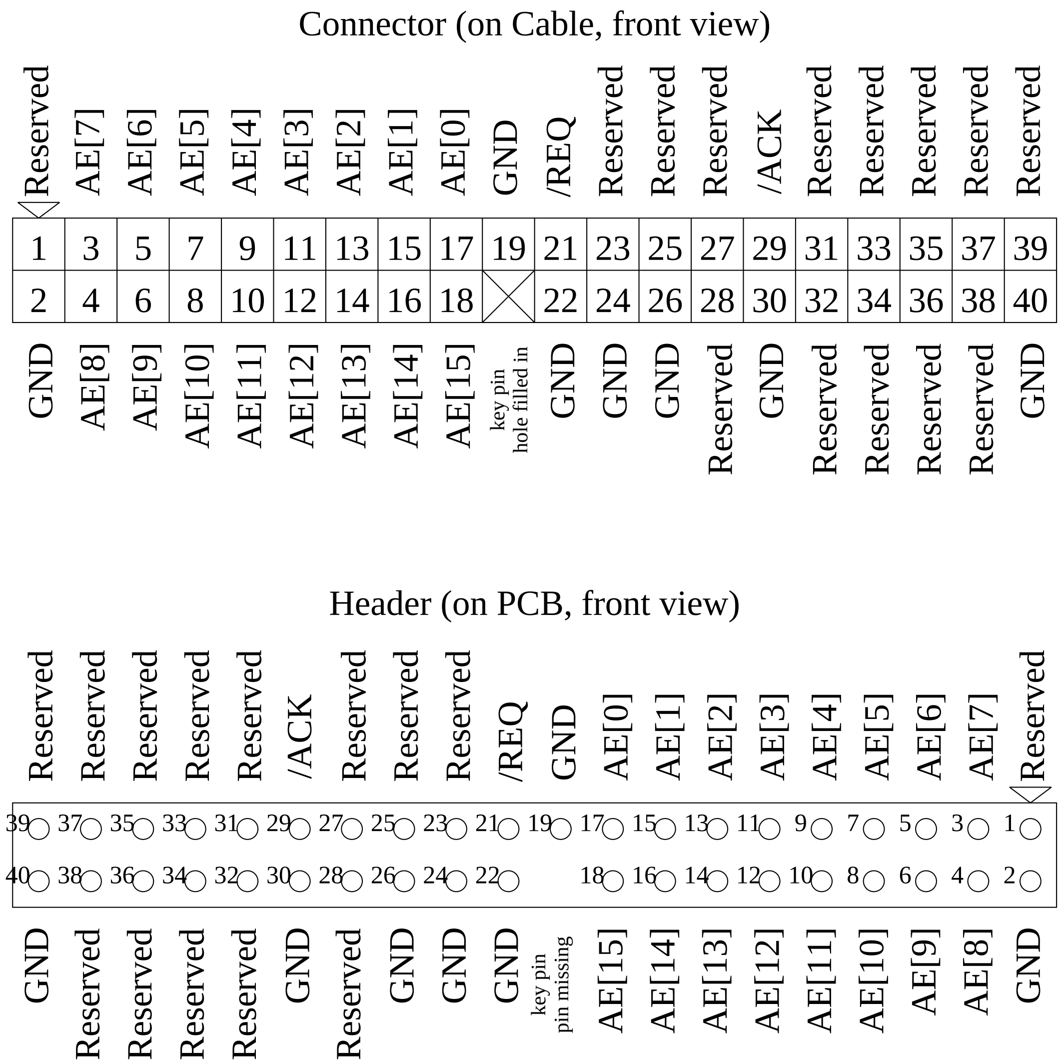

Figure 1: IDC 40 plugs for ATA/133 based AER bus standard

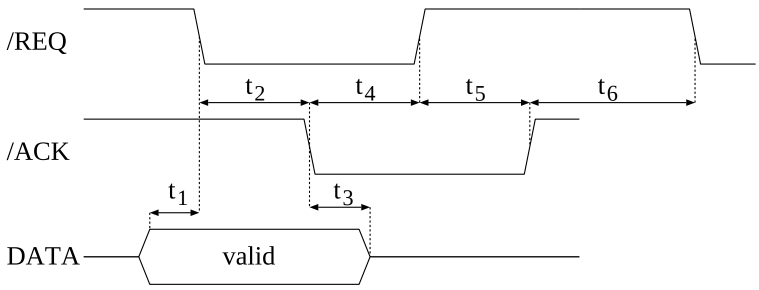

Figure 2: 4 phase handshake. Timing constraints in table 2.

	min	max	avg
t_1	0s	∞	
t_2	0s	∞	$\leq$ 700ns
t_3	0s	∞	
t_4	0s	100ns	
t_5	0s	100ns	
t_6	0s	∞	

Table 2: Timing requirements of 4 phase handshake (figure 2)

2 Package protocol and signal timing diagram

The asynchronous transmission protocol for the single-sender/single-receiver AEs is a 4-phase handshake. The digital signal levels are 3.3V (high) and 0V (low). The standard TTL margins for high and low signals apply. Signal transition times should be below 10ns for the capacitive load of a bus cable, say typically well below 0.1nF. In other words the output current driving the transition (named short cut current in some data books) should be about 50mA. The usual causal rules for /REQ, /ACK and DATA (this is the address in AER) apply (figure 2). The causal order of the signals has to be maintained, i.e. all times in the figure need to be bigger than 0 (table 2). /REQ and /ACK are active low.

The upper time limits result from assumptions that determine the necessary bus bandwidth as follows: The biggest address space (in the CAVIAR project) is the one used by the retina/imager chip, which might achieve a resolution of up to 128x128 pixels. That would correspond to a 14 bit address space, i.e. 16384 addresses. If we limit the firing frequency range for a pixel to maximal 100Hz and if we assume that never more than half the pixels will be active, then we can conclude that an AER bus needs to transmit never more than 819200 events per second. Thus one transmission can be allowed to last up to approximately 1μs. The timing requirements for t_4 and t_5 in table 2 ensure that a transmission lasts but 200ns once both partners have agreed to transmit. It is very desirable that our devices will be even faster than those upper limits. The *avg* requirement for t_2 ensures that the average total transmission time is below 900ns. The receiver is however allowed to put the sender on hold longer than that in individual cases. This might be unavoidable for some time when the receiver is an AER remapper that merges several inputs. All other devices should aim at having this delay shorter than 100ns.